AMENDMENTS TO THE CLAIMS

(IN FORMAT COMPLIANT WITH THE REVISED 37 CFR 1.121)

1. (CURRENTLY AMENDED) A method for generating a superset pinout for a family of devices having potential footprint variations, comprising the steps of:

(A) defining a pinlist for each device within said family of devices;

(B) generating a superset listing of pins from said pinlist;

(C) creating said superset pinout for said family of devices from said superset listing of pins to eliminate said potential footprint variations within said family of devices; and

(D) marking each pin of said superset pinout associated with each member of said family of devices.

2. (PREVIOUSLY PRESENTED) The method according to claim 1, wherein step (D) further comprises;

customizing a superset grid according to said superset listing of pins.

3. (CURRENTLY AMENDED) The method according to claim 2, wherein ~~step (D) further~~ said customizing comprises:

marking a specific pin in said superset grid for each member of said family of devices ~~in response to the customizing~~.

4. (ORIGINAL) The method according to claim 1, wherein said family of devices comprises devices with combined programmable logic and high-speed serial channels.

5. (CANCELED)

6. (PREVIOUSLY PRESENTED) The method according to claim 1, wherein step (C) further comprises:

eliminating potential layout variations within said family of devices with said superset pinout.

7. (PREVIOUSLY PRESENTED) The method according to claim 1, wherein step (B) further comprises:

combining pins shared by more than one member of said family of devices.

8. (ORIGINAL) The method according to claim 1, wherein step (C) further comprises:

allocating a pin for each signal in said pinlist.

9. (CURRENTLY AMENDED) The method according to claim 1, wherein step (C) further comprises:

providing a common footprint ~~to~~ for each member of said family of devices.

10. (CURRENTLY AMENDED) The method according to claim 1, wherein step (C) further comprises:

designing a board layout (i) to accommodate more than one member of said family of devices and (ii) to allow for ~~late~~ later changes from one member of said family of devices to another member of said family of devices without affecting said board layout and without external components.

11. (PREVIOUSLY PRESENTED) The method according to claim 1, wherein step (C) further comprises:

limiting each pin of said superset pinout to a single function.

12. (CANCELED)

13. (ORIGINAL) The method according to claim 1, wherein step (D) further comprises:

marking one or more pins no-connect for a particular member device.

14. (ORIGINAL) The method according to claim 1, wherein said family of devices comprise programmable logic and high-speed serial channel devices.

15. (ORIGINAL) The method according to claim 1, wherein step (C) further comprises:

allowing for migration of devices within said family of devices.

16. (ORIGINAL) The method according to claim 1, wherein step (C) further comprises:

allowing for migration to higher gate densities.

17. (ORIGINAL) The method according to claim 1, wherein step (C) further comprises:

allowing for migration to increased bandwidth channels.

18. (PREVIOUSLY PRESENTED) The method according to claim 1, wherein step (C) further comprises:

reducing layout and footprint changes on a board configured to connect to said members of said family of devices.

19. (CURRENTLY AMENDED) An apparatus for generating a superset pinout for a family of devices having layout variations comprising:

means for defining a pinlist for each device within said family of devices;

means for generating a superset listing of pins from said pinlist;

means for creating said superset pinout for said family of devices from said superset listing of pins, wherein said superset pinout eliminates said layout variations within said family of devices; and

means for marking each pin of said superset pinout associated with each member of said family of devices.

20. (CURRENTLY AMENDED) An apparatus comprising:

a device configured to generate a superset pinout for a family of devices having layout and footprint variations, wherein (A) said device is further configured to (i) define a pinlist for each device within said family of devices, (ii) generate a superset listing of pins from said pinlist, (iii) create said superset pinout for said family of devices from said superset listing of pins, and (iv) mark each pin of said superset pinout associated with each member of said family of devices, and (B) said superset pinout is configured to reduce layout and footprint changes on a

board configured to connect to each member of said family of devices.